Wide Band Systems, Inc.®

Technical Product Bulletin No. 104

DIGITAL FREQUENCY DISCRIMINATORS

WIDE BAND SYSTEMS' Digital Frequency Discriminators (DFD) are integrated microwave/video/digital assemblies which provide digital encoding of wide band RF input signal frequency data for pulsed or CW RF signals. In addition to encoding of RF frequency, DFDs can also provide a threshold based on the instantaneous RF Signal to Noise Ratio (SNR), Error Detection, and various flag functions including Out Of Band, Frequency Modulation On Pulse (FMOP), and Phase Modulation On Pulse (PMOP). The DFD is an essential component of an IFM Receiver.

The DFD basic structure

All WIDE BAND SYSTEMS' DFD designs employ an RF limiting amplifier, a DC coupled parallel array of microwave correlators with delay lines in a binary (1, 2, 4, 8,…) sequence, and a TTL/CMOS digital decoder circuit card assembly. Neither DC Restoration nor ovens are employed; temperature correction of delay line thermal drift is accomplished by measurement of the delay line temperature, then digital correction of the output data.

MINIATURE DFD

The RF amplifier

A single RF limiting amplifier is necessary for the DFD to stabilize the video levels for decoding. Additional RF limiting amplifiers may be employed either external or internal to the DFD to achieve the required RF dynamic range.

The correlator array

The parallel array of microwave correlators with delay lines arranged in a binary sequence has been shown to be the most powerful frequency decoding algorithm in current production, in terms of operation at low RF SNR and in the presence of simultaneous RF signals which are closely spaced in time and RF level. The DFD is provided with an analytically generated digital Error Correction Algorithm, allowing any or all correlators to be in error by ±45 electrical degrees.

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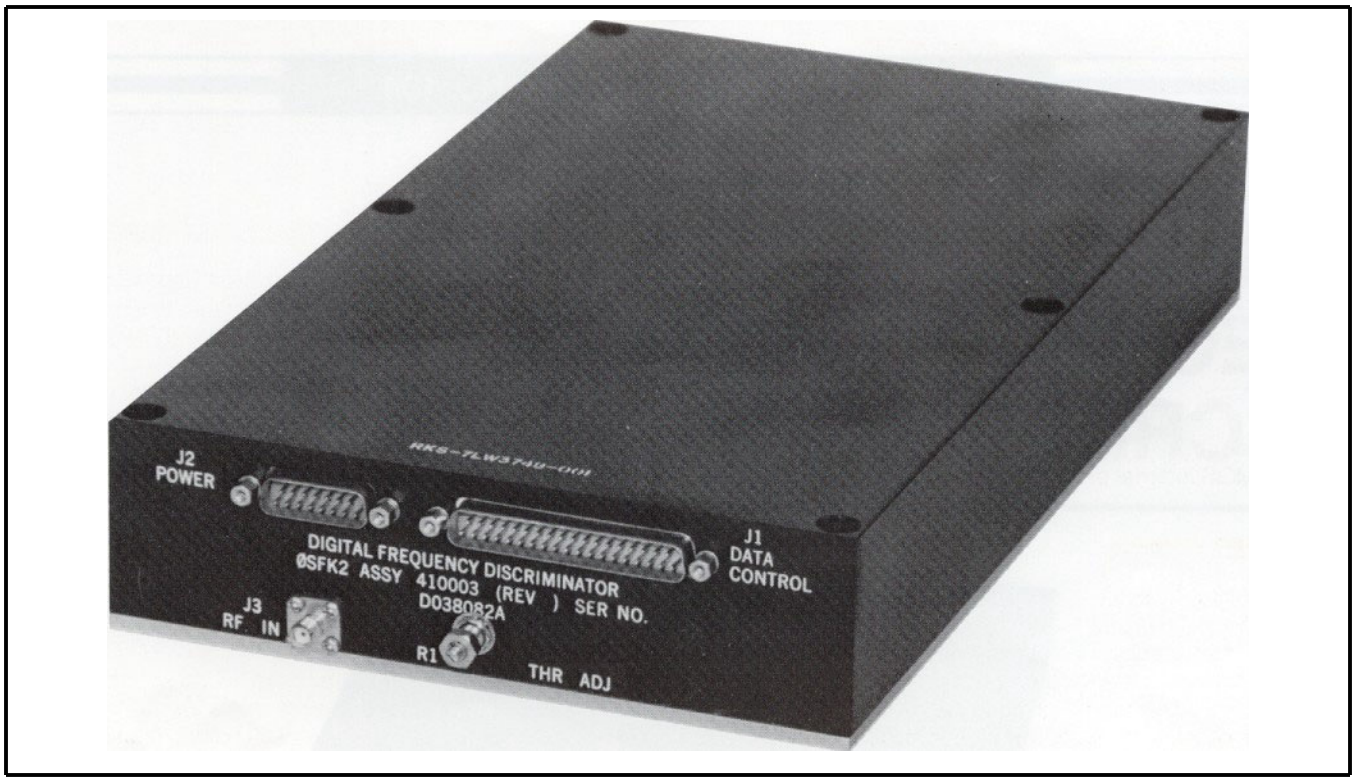

STANDARD DFD

How many correlators?

The number of correlators employed in a DFD varies with the application, with a typical design employing seven correlators to produce a twelve or 13 bit digital output. Designs have been produced with as few as four correlators and as many as ten correlators, to realize specific system performance objectives. In any design, the longest delay line correlator establishes the RF frequency measurement accuracy and resolution; the shortest delay line correlator defines the unambiguous bandwidth of the DFD; the remaining correlators serve only to resolve the ambiguities between these two correlators. In some applications (usually those in conjunction with an RF Channelizer) the DFD design may be ambiguous over the operating bandwidth; normally, however, the unambiguous bandwidth exceeds the operating bandwidth. The RF frequency measurement decoding process provides multibit digitization only on the longest delay line correlator; the other correlators are provided only with signum function quantization. Considering that the binary relationship between delay lines provides a complete orthogonal basis in the multibit sine/cosine space, further quantization of these correlator outputs will provide no additional information.

A parallel processor

The general sequence of RF frequency encoding is to digitize the parallel sine/cosine video signals from the correlator array, simultaneously apply the Error Correction and Error Detection algorithms to the resultant digital data, then temperature correct the digital output data. The Flag processing (Out of Band, FMOP, PMOP, and Coherent Threshold) is accomplished in parallel.

External/internal triggering

The DFD may be either externally or internally triggered; many units are provided with both capabilities, with external selection of the trigger source. The trigger processing may be either a one-shot latch and hold sequence or a clocked sequence. The one-shot latch and hold sequence requires either an external trigger pulse or, internally, either an RF amplitude based threshold circuit, employing a detector, or an RF SNR threshold, employing the Coherent Threshold. Once a trigger is received (or generated) by the DFD, a cycle takes place and the digital data is presented to the interface. The one-shot latch and hold sequence provides the fastest response time, from trigger input to data output, in terms of elapsed time. The DFD is usually provided with a handshake circuit with the external processor, with a Data Ready Strobe indicating that new RF frequency data is on the interface, and requiring a Data Acknowledge input to allow a new conversation to take place.

Clocking – an alternative

As an alternative to the one-shot latch and hold sequence, the DFD may employ a clocked sequence, at clock rates up to 40MHz. The clocked sequence employs either an internal or external clock circuit, making a frequency measurement once every clock cycle. While the one-shot latch and hold sequence provides the fastest time from trigger input to data output, the clocked sequence can sustain the highest throughput rate (in terms of RF frequency measurements per second), and has the smallest shadow time. The shadow time is the required time interval between RF frequency measurements; the clocked design has the smallest shadow time because new data can be clocked in while the old data is being clocked out, in a pipeline process. The 40MHz clock rate limitation is due to the TTL/CMOS internal processing circuits.

External clock

External clock rates up to 40MHz are supported; in this mode, the DFD provides RF frequency and flag data a specific number of clock cycles (usually seven) delayed from the RF input. The external clock rate may vary over a wide range (up to 40MHz), with the number of clock cycles to the output being fixed; if the clock is stopped, the data is held in the DFD until the clock restarts. The external clock mode is often employed with synchronous switching of the host system RF band and/or with synchronous antenna switching. There is usually no handshake; the clock which triggers the DFD is also employed to read the DFD output data. WIDE BAND SYSTEMS' IFM Receivers employ a 40MHz clock for RF frequency data; this clock is also employed to produce RF amplitude digitization synchronously with RF frequency digitization.

Internal clock

Internal clocking of a DFD is usually employed in conjunction with the Coherent Threshold and Associative Processor to provide a leading edge pulse-on-pulse and pulse-on-CW trigger capability. In this mode, the DFD measures both the RF frequency and the RF SNR on every sample, at a 40MHz rate. The Coherent Threshold provides a signal present indication, based on RF SNR (as opposed to RF amplitude); the Associative Processor examines each measurement to determine whether the same, or a similar, RF frequency has been previously observed within the pulse (or CW) envelope. The resultant DFD detects both pulse-on-pulse and pulse-on-CW events, provides a leading edge trigger, and suppresses the response to both RF multipath and broadband noise inputs. The full dynamic range recovery time of this process is 50nS, limited by the digital processing circuits; neither SDLVA's nor VVA's are employed. As noted, the one-shot latch and hold sequence provides the shortest conversion time; this sequence is also effective with very short (15nS) RF pulse widths. The clocked sequence provides the highest throughput rate of data, but is limited in the minimum RF pulse width that can be processed. A 20MHz clock rate is limited to minimum RF pulse widths of 100nS, with a degradation of Probability of Intercept (POI) to approximately 30% at a 50nS RF pulse width. The 40MHz clock rate provides a 100% POI, for 50nS RF pulse widths, degrading to approximately a 15% POI at a 25nS RF pulse width.

Many configurations available

In addition to a wide range of available design variations with respect to RF frequency coverage, measurement accuracy and resolution, trigger source, processing sequences, and threshold circuits, WIDE BAND DFDs are provided in two basic packages. The standard package employs separable stripline microwave components and a circuit card assembly; typical sizes include 7 x 12 x 2 inches (178 x 305 x 51mm). The integrated package employs a single stripline package with all microwave circuits, plus a circuit card assembly; typical sizes include 5 x 5 x 0.5 inches (127 x 127 x 13mm). Examples of the two packages are illustrated.

Reliability through design

Because reliability is substantially dependent on device temperatures, considerable care has been taken to minimize the power consumption of each DFD design, and attention has been given to conductively cooling each active component. RF amplifiers are directly attached to the heat transfer surface; digital components are conductively cooled via thermal pads placed on a copper sheet, which is thermally attached to the DFD housing. All logic elements are TTL/CMOS; ECL circuits are used as TTL/ECL converters only in those applications where an ECL interface is required. Operating voltages are either +12VDC or +15VDC, employed only with the RF amplifiers; +5VDC services the TTL/CMOS logic; -5.2VDC to -6VDC is employed as a bias source. DC power requirements are typically less than 20W, with 1A at +5VDC, 0.3A at -5.2VDC, and the balance dependent on the required RF gain in the RF limiting amplifier.

Technical support services

WIDE BAND SYSTEMS offers a large variety of DFD configurations and processing approaches within a defined RF processing bandwidth. The technical staff at WIDE BAND SYSTEMS stands ready to assist in system definition and integration, and will continue to support the design through the service life of the system. We maintain an extensive library of proprietary software programs to predict system performance with a DFD, including measurement accuracy versus RF SNR, threshold performance versus RF SNR, and others, for a variety of DFD design configurations.

WIDE BAND SYSTEMS' DFD designs represent the state of the art in the precision measurement of RF frequency, and are the culmination of more than 20 years of incremental design improvements to the basic binary correlator DFD. The Coherent Threshold and Associative Processor circuits are both unique to WIDE BAND SYSTEMS, Inc. and are U.S. Patent Pending.

How to get more information

For additional technical information on Wide Band Systems' Digital Frequency Discriminators, including performance data on specific models, or to discuss your application in detail, please get in touch with us today. We will respond to your inquiry promptly.

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