

LEADING-EDGE THRESHOLD CIRCUIT AIDS DFD ACCURACY

Short-duration, high power RF pulses can be detected within long pulses or continuous-wave signals.

DIGITAL frequency discriminators (DFDs) are employed in a variety of electronic-warfare (EW) systems to provide accurate digital frequency data on received pulsed and continuous-wave (CW) RF signals. By employing the proper leading-edge triggering scheme, a DFD can detect and process pulse-on-pulse and pulse-on-CW signal events at high data rates.

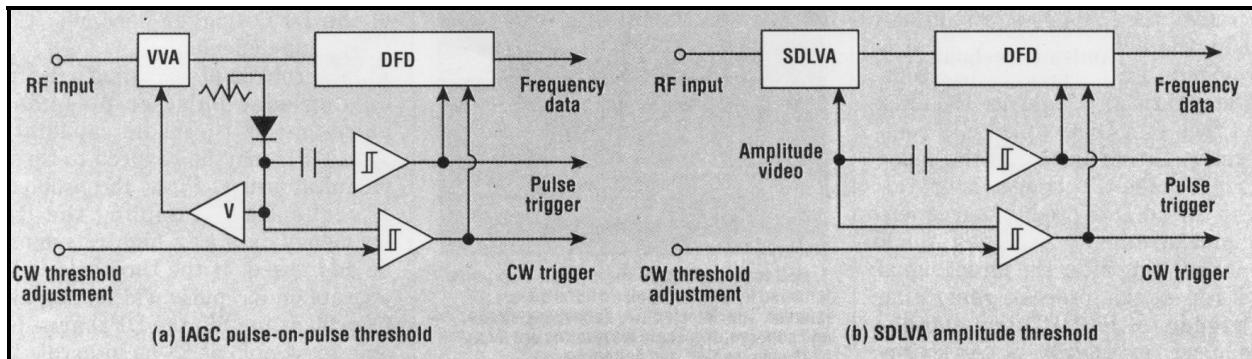
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Characteristics of the modern DFD include instantaneous frequency coverage that can span multiple octaves in the microwave band and instantaneous dynamic ranges in excess of 60 dB. Various designs have been developed to provide accurate frequency data on RF pulse widths as short as 10 ns, with typical designs providing 50-ns-to-CW coverage. The modern DFD is a fast digital encoder capable of processing and outputting measured data at a rate that can exceed four million RF pulses per second.

The DFD, by its nature, is a serial data processor, providing measured frequency data on the strongest signal observed within the RF bandwidth. CW and long RF pulse widths, therefore, can "capture" the DFD, often preventing the observation and measurement of other RF signals that may be simultaneously present. In the

event that a simultaneous signal is of a higher RF power than the initial RF input, the "capture" problem can be reduced if the DFD has the ability to detect the presence of a measurable simultaneous RF input, then performing the frequency measurement of the simultaneous signal subsequent to measurement of the initial RF input.

The utility of a DFD capable of detecting and processing pulse-on-pulse and pulse-on-CW signal events may be offset by the inability of the host-system processor to accommodate the higher data rates that can result. The impact of the higher digital data rates can be minimized by providing a leading-edge trigger capability where, for example, if a short-duration, high-power RF pulse is received during a longer-duration, low-power RF pulse, the DFD will respond sequentially to the two pulses. That is, the DFD will respond to the



1. Two methods for providing leading-edge threshold capability involve instantaneous AGC (a) and SDLVA circuitry (b).

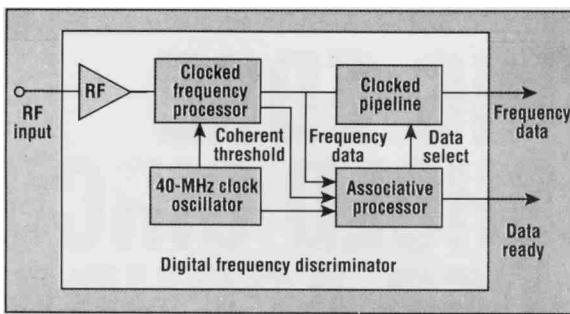
DFD TRIGGERING

frequency data on the initial signal, then to the frequency data on the short-duration signal while suppressing a subsequent report which would repeat the initial frequency data.

In a multipath environment, an RF signal is received first over the direct path from the emitter, then subsequently over one or more indirect paths caused by reflections from objects or surfaces located off the direct path. The multipath reflected signal is always at the same frequency as the direct-path signal (except for Doppler effects, which can usually be ignored) but presents an RF amplitude that may be different. The leading-edge trigger capability tends to suppress the effect of RF multipath, as equal-frequency signals received subsequent to the direct path are ignored. Further, if RF amplitude measurements are triggered by the DFD for the purpose of amplitude-comparison direction finding, the leading-edge trigger circuit will suppress angular measurement errors for all scenarios except a small geometric area known as the error-susceptibility region.

A number of approaches have been used to meet these objectives. For instance, one technique employs a voltage-variable attenuator (VVA) as part of a fast, low-gain, instantaneous automatic-gain-control (IAGC) loop. This loop is designed to provide an output-RF-level variation of approximately 15 dB for a 70-dB variation in input RF level.

In operation, a long-duration RF input is read by the detector. The detected video output is then provided to a fast video amplifier, which increases the VVA loss. Simultaneously, the detected video signal is provided to a pulse threshold comparator through a highpass RC filter and then to a DC-coupled CW comparator. Either (or both) the pulse trigger or the CW trigger is provided to the DFD to produce a frequency measurement. A stronger RF input arriving after the initial signal will repeat this process, generating a trigger to the DFD and another frequency measurement. An external voltage is required for the CW threshold reference to allow the processing of slow-rise-time



2. This DFD architecture features an associative processor block, which can determine whether the present frequency sample is due to a new or previously-detected signal.

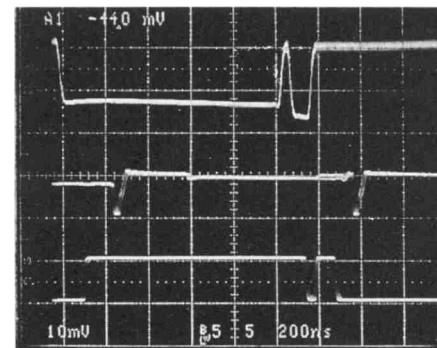
RF signals.

While the IAGC threshold circuit (Fig. 1a.) was largely effective in providing the appropriate trigger responses for the DFD, there were some drawbacks. First, the threshold circuit's recovery time from strong signals was poor, requiring almost a microsecond to return to full sensitivity. Second, the process of thresholding frequency data based on amplitude measurements has an inherent flaw in that it is assumed that merely because there is a measurable amplitude difference, there will also be measurable frequency data. This problem is particularly acute when there is substantial RF gain between the VVA and DFD, as the small-signal gain variation of an RF amplifier will add to the amplitude margin required to provide a useful trigger. Since the setting of the CW threshold is based on the noise-level input to the DFD, a band-switched RF front end requires a programmable voltage input to accommodate the RF-

noise-level variation as the RF input band is switched.

The sequential-detector-logarithmic-video-amplifier (SDLVA) threshold circuit (Fig. 1b) can also provide a leading-edge threshold capability for the DFD. In this approach, the SDLVA produces a voltage output which is proportional to the logarithm of the RF input-power level.

This method has the advantage of providing RF amplitude data along with frequency data, with the circuit recovering faster than the IAGC threshold. Unfortunately, it suffers from the basic problems of employing RF amplitude data to trigger an RF frequency measurement, as well as having a variable CW threshold. In addition, the basic process of resolving a pulse-on-pulse threshold level with this logarithmic technique is mathematically different from the square-law detection and threshold process of Fig. 1a. Also, the SDLVA has an inherent variation of the log-video-output timing related to the RF input power level. This can cause problems in the measurement of short RF pulses because the timing of the DFD trigger becomes RF-amplitude-dependent. The problem of providing a useful leading-edge pulse-on-pulse and pulse-on-CW threshold capability for a DFD may be reduced to three technical issues. First, the problem of sequentially sampling the RF frequency data at a high rate must be addressed. If the threshold is to operate on RF pulse widths ranging from 50 ns to CW, the DFD must be able to sample at 25-ns intervals to assure (given the video settling-time requirements and effective RF-pulse-width loss due to



3. DFD recovery time is shown for a 1-μs pulse followed by a 100-ns pulse after a 50-ns interval. The detected-RF, data-ready-strobe, and coherent-threshold waveforms are depicted by the top, center, and bottom traces, respectively.

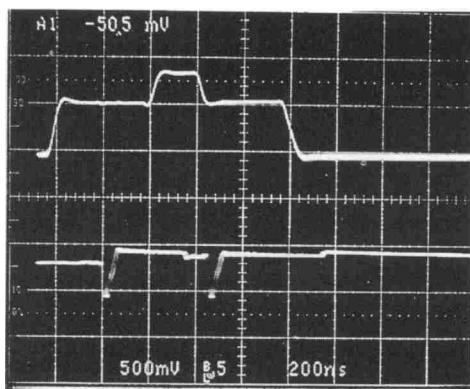
DFD TRIGGERING

delay lines) that at least one valid frequency measurement is obtained for each RF input signal. This requires the DFD to clock data at a 40-MHz rate.

Second, the validity of each measured frequency sample must be determined on a sample-by-sample basis. This validity question takes two forms: first, the signal-to-noise ratio (SNR) must be estimated for each frequency measurement sample; second, given that a sufficient SNR exists, the measurement validity must be determined. The first task can be accomplished by the coherent threshold circuit developed by Wide Band Systems, Inc. (Franklin, NJ). This circuit provides a sample-by-sample estimate of the SNR observed by the frequency-measurement process. Since the coherent threshold output is only a function of the SNR, the DFD can determine the threshold (in terms of the RF SNR) independently of the external noise-power level. The second task is accomplished on a sample-by-sample basis by the SSD function.

The third major technical challenge involves a frequency sample obtained in 25 ns, with the sample having a sufficient SNR to provide useful frequency data and being free from errors due to, for example, a simultaneous signal at approximately the same RF input level. Given these conditions, it must be determined whether the sample is due to a new signal. The problem becomes complex since the frequency being sampled may correspond to a previous RF input while there may have been other frequencies present in the intervening period, such as would occur if a short-duration, high-power RF input is present during a long-duration, low-power RF input. The DFD must recognize that the frequency measurement which follows the short-duration signal is similar to (but not necessarily identical to) the measurement that occurred prior to the short-duration signal. The technical objective is achieved by the associative processor, which is a digital circuit that can quickly recognize that the present frequency digital sample is similar to a previous (but not necessarily time-contiguous) frequency sample.

Figure 2 is a block diagram of the



4. DFD response to a typical pulse-on-pulse situation is shown. The video-amplitude and data-ready traces are shown at the top and bottom, respectively. ■

DFD. The RF input is amplified to produce hard limiting over the full dynamic range. A 40-MHz clocked processor generates a digital frequency sample every 25 ns. Each sample includes a coherent threshold tag, with the stream of frequency samples clocked through a pipeline circuit. The associative processor is active whenever the coherent threshold indicates that an above-threshold signal is present. When the associative processor determines that a new RF input is present, the appropriate sample is selected in the clocked pipeline for output and a data-ready strobe is issued. The circuit ignores data resulting from simultaneous signal errors.

A working DFD with these characteristics has been produced. The DFD operates from 7.5 to 18 GHz with 3-MHz resolution over an RF dynamic range of -60 to +10 dBm using an internal RF limiting amplifier. Figure 3 demonstrates the DFD recovery time, showing a 0-dBm, 1- μ s RF pulse followed by a -60-dBm, 100-ns RF pulse with a 50-ns interval in between the pulses. The interval was provided for illustration purposes, as the DFD only requires that the second signal exist for more than 50 ns beyond the strong signal.

Figure 4 presents the DFD response to the classic pulse-on-pulse situation, providing one data-ready output for each

RF input event. The short-duration RF pulse was 6 dB stronger than the long-duration RF pulse. The DFD output data-ready port was connected to the DFD-input data acknowledge, causing a very short data-ready strobe width.

This DFD uses a digital technique to provide leading-edge pulse-on-pulse and pulse-on-CW threshold triggering. This eliminates the need for VVAs, SDLVAs, and external CW threshold voltage references, as the DFD threshold is instantaneously self-adaptive to the current RF SNR. The circuits employed are entirely digital, using "F"-series TTL logic. The DFD was tested over a temperature range of -54 to +85°C. The 7.5-to-18-GHz DFD uses a standard 7 X 12 X 12 in. (17.8 X 30.5 X 30.5 cm) package, while the 2-to-6-GHz version employs a 7.3 X 6.2 X 0.6 in. (18.5 X 15.7 X 1.5 cm) miniature package. Other bands and physical configurations are available. ••

How to get more information

For additional information on leading-edge threshold capability as it relates to Wide Band Systems' Digital Frequency Discriminators, performance data on specific models, or to discuss our application in detail, please get in touch with us today. We will respond to your inquiry promptly.



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