

Technical Bulletin

SUMMARY OF SPECIFICATIONS **Digital Frequency Discriminator 0.5–18.0GHz**

ELECTRICAL OPERATING SPECIFICATION

Frequency Measurements Requirements

| | |
|-------------------------------------|----------------------|
| Operating Frequency Range | 0.5-18.0GHz |
| Unambiguous Bandwidth | 20.48GHz |
| Mean Frequency Resolution | 1.25MHz |
| Digital Frequency Resolution | 14Bits |
| Frequency Accuracy | 3.0MHz RMS |
| Peak Error | 15.0MHz |
| Signal Level Range | -55 to +15dBm |

Pulse Width Range 100ns to CW

Minimum Input S/N Ratio +3dB minimum for full accuracy

Maximum RF Input Power +17dBm CW maximum (no damage)

RF Input VSWR 2.0 : 1 typical

TIMING REQUIREMENTS

Throughput Time The time from when the RF enters the DFD until a DATA READY indication must be 200 ns maximum

Recovery Time The unit must recover to full sensitivity within 100ns after the end of a CW input at +10dBm.

Processing Blind Time The unit must process two separated pulsed signals when the time between the leading edge of DATA ACKNOWLEDGE and the leading edge of the subsequent SIGNAL

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Signal Present Timing

PRESENT is greater than 50ns

The time from when the RF enters the DFD until a SIGNAL PRESENT indication is issued must be 150ns maximum

Data Ready Timing

The time from when a SIGNAL RESENT indication is issued until a DATA READY indication is issued must be 50 ± 10ns

Duty Cycle

The combination of pulse width, pulse amplitude, or duty cycle cannot cause a false generation of either a DATA READY or SIGNAL PRESENT output

INPUT/OUTPUT INTERFACE

Control Input Logic Requirement

TTL compatible

Data Acknowledge

Logic HIGH = normal state. When DATA ACK transitions to logic "L" state, the output data must be held in the output registers until the DATA ACK returns to logic "H" state. Pulse width of DATA ACKNOWLEDGE must be 50 ns to 100ns

Read Select

Logic HIGH selects INTERNAL MODE

LOW selects External Mode

External Read

Logic HIGH = normal state. When transitions to logic "L" state, activates the reading of RF signal which is present.

Pulse width of the command shall be 100 nsec. to 150 nsec. DATA READY shall not be issued without SIGNAL PRESENT or CW ALARM active during EXTERNAL READ

Output Logic Requirement

TTL compatible

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| | |
|--------------------------------|--|
| Frequency Data | 14 bit binary active HIGH |
| Fast Signal Present | Logic LOW < 100nsec. From RF Input leading edge |
| Coherent Signal Present | Logic LOW < 150nsec. From RF Input leading edge |
| Data Ready | Logic HIGH initially changing to logic LOW when frequency data has settled and returning to logic HIGH when DATA ACKNOWLEDGE is supplied to DFD |
| Out Of Band Flag | Logic LOW when RF Input is frequency more than 550MHz above or below band edge |
| FMOP | Active LOW when the rate of change of the RF Input frequency exceeds 5MHz per 25nsec. Requires a minimum 200nsec RF pulse to activate |
| CW Flag | Active LOW when RF input pulse width exceeds a preset limit |
| Data Invalid Flag | Active LOW |

MECHANICAL SPECIFICATIONS

| | |
|----------------------------|---|
| Physical Dimensions | 7in. X 10in. X 3in. |
| Weight | 8lbs. maximum |
| Cooling | Conduction cooling at mounting surface |
| RF Input Connector | SMA Female |
| Power Connector | MDM9P |
| Control Connector | MDM51S |
| POWER | |
| DC +15 V ± 5% | 1.4 A maximum |

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DC +5 v \pm 5%

DC -5.2 v \pm 5%

1.0 A typical

2.0 A maximum

1.5 A typical

600 mA maximum

400 mA typical

ENVIRONMENTAL CONDITIONS

Temperature

Storage Environment -40° C to +85° C

Mounting Surface (operating) -40° C to +80° C

Vibration MIL-STD 202F Method 204D Condition B, (15G, 10Hz -2KHz)

Shock MIL-STD-202G Method 213B Condition B, (75G, 6ms, Half-sine)

Humidity MIL-E-5400T 3.2.24.4 (100% R.H.)

Altitude MIL-E-5400T Table VIII (55,000 ft.)

WARRANTY

Wide Band Systems, Inc. warrants against DFD deterioration of performance specified above for twelve (12) months after delivery, except in the case of failures attributed to the user.

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